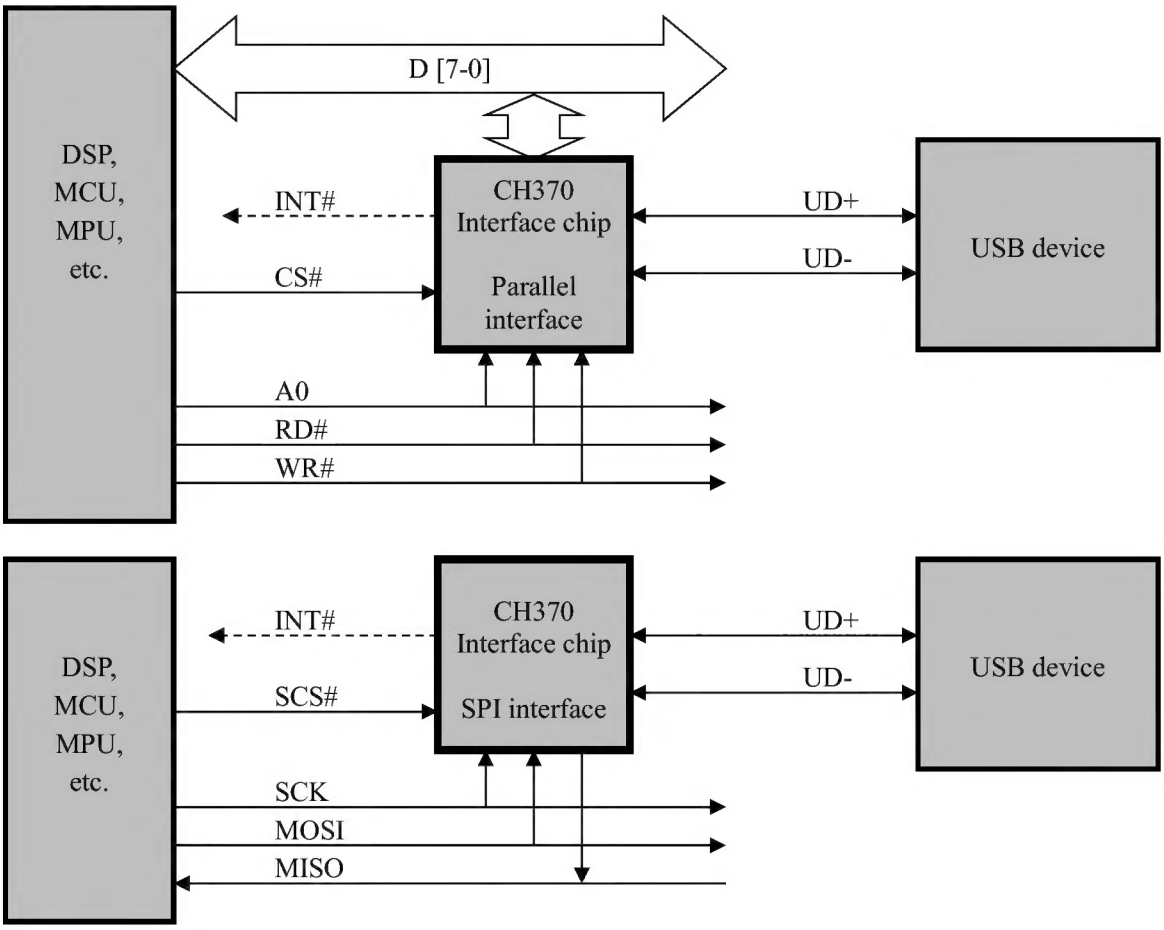
USB-Host Interface Chip CH370

Datasheet
Version: 1B
http://wch.cn

1. Overview

CH370 is a host interface chip of USB bus which supports low-speed and full-speed control transmission, bulk transmission and interrupt transmission. With the interface of controller such as DSP/MCU/MPU, it supports 8-bit parallel bus and 4-wire or 3-wire SPI serial bus.

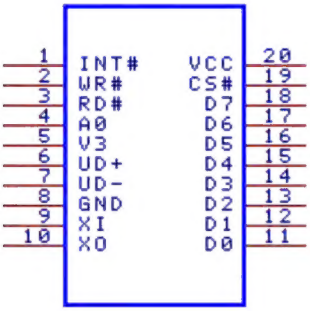


2. Features

- Support 1.5Mbps low-speed and 12Mbps full-speed USB communication, compatible with USB V2.0.
- Support commonly used low-speed and full-speed USB device control transmission, bulk transmission and interrupt transmission.
- Automatically detect the connection and disconnection of USB device, and provide interrupt notifications for device connection and disconnection.
- Built-in impedance match series resistor of the USB signal line and the built-in pull-down resistor of the USB host terminal.
- Two MCU interfaces are optional: 8-bit passive parallel interface at the speed of 5MB and SPI serial interface at the speed of 3MB/24MHz.
- The SPI serial interface includes SPI chip selection, serial clock, serial input and output, and SPI output and input can be connected in parallel.

- The interrupt output pin is an optional connection and is active at low level. It can be replaced by querying the interrupt flag bit in the register.
- Support 5V supply voltage and 3.3V supply voltage, and having a function of built-in power-on reset. CH370V only supports 3.3V supply voltage.
- SSOP-20 lead-free package, and compatible with RoHS.

3. Package



Package	Width of plastic		Pitch of pin		Instruction of Package	Ordering information
SSOP-20	5.30mm	209mil	0.65mm	25mil	Subminiature 20-pin patch	CH370T
SSOP-20	5.30mm	209mil	0.65mm	25mil	Subminiature 20-pin patch	CH370V

Note: CH370V only supports 3.3V supply voltage, CH370T supports 5V supply voltage and 3.3V supply voltage.

4. Pins

Pin No.	Pin Name	Pin Type	Description
20	VCC	Power	Positive power input, an external 0.1uF power decoupling capacitor is required
8	GND	Power	Common ground, required to be connected to the ground wire of the USB bus
5	V3	Power	Connected to the VCC input external power source at the supply voltage of 3.3V Connected to an external 0.1uF decoupling capacitor at 5V supply voltage
9	XI	Input	Input terminal of the crystal oscillator, required to be connected to an external crystal and oscillation capacitor
10	XO	Output	Inverted output terminal of the crystal oscillator, required to be connected to an external crystal and oscillation capacitor
6	UD+	USB signal	USB bus D+data line
7	UD-	USB signal	USB bus D - data cable
18～11	D7～D0	Bi-directional Tri-status	8-bit bidirectional data bus, built-in weak pull-up resistor D3 is also the SCS# of the SPI interface, D5 is also the SCK of the SPI interface, D6 is also the SDI of the SPI interface, D7 is also the SDO of the SPI interface.

3	RD#	Input	Read strobe input, active low, built-in pull-up resistor
2	WR#	Input	Write strobe input, active low, built-in pull-up resistor
19	CS#	Input	Chip selection control input, active low, built-in weak pull-up resistor
1	INT#	Open-drain output	Interrupt request output, active low, built-in pull-up resistor
4	A0	Input	Address line input, distinctive index port and data port, built-in weak pull-up resistor

5. Register

The MCU referred to in this datasheet is basically applicable to DSP or SCM/MCU/MPU/CPU, etc.

The internal register and buffer area of CH370 are allocated in the address range from 00H to 0FFH, and are accessed after being addressed by the MCU.

The default value after reset is expressed in binary number, and its characteristics can be described by several character flags, which are as follows:

0: Always 0 after reset;
1: Always 1 after reset;
X: This bit is automatically set by internal hardware or affected by the status of external pins;
=: Reset does not affect the data, and the initial value of the data is uncertain;
?: Reserved bit; the read data has no meaning. You must write 0 or 1 or keep the original value when writing.

Address range Hexadecimal system	Register name (marked in gray) Bit name of register	Register description (marked in gray) Bit description of the register	Default value after software /hardware reset
00H-03H	Reserved	Disable reading and writing	????????
04H	REG_SYS_INFO	System information register, read only	XXX?XX01
04H bit 7	BIT_INFO_POWER_RST	Completion status of hardware power-on reset: 0=resetting; 1=reset completed	0/X
04H bit6	BIT_INFO_WAKE_UP	The chip wake-up status is not affected by software reset: 0=sleeping or waking up; 1=woken up	X
04H bit 5	BIT_INFO_SOF_PRES	Hardware 1mS timing cycle status, 1= SOF packet will be generated	=/X
04H bit 4	Reserved	The data read is meaningless and uncertain	?
04H bit 3	BIT_INFO_USB_DP	Logic level state of USB bus UD+ pin	X
04H bit 2	BIT_INFO_USB_DM	Logic level state of USB bus UD- pin	X
04H bit 1 04H bit 0	Hardware identification bit	Fixed value, always constant 01, Used to verify that the hardware connection is correct and the read operation is successful	01
05H	REG_SYS_CTRL	System control register, not affected by the software reset	00000000
05H bit 7 to 05H bit 4	It must be 0100	The data read is meaningless and must be 0100	0000

05H bit 3	BIT_CTRL_RESET_NOW	Chip software reset control: 0=no reset; 1=reset	0
05H bit 2	BIT_CTRL_USB_POWER	USB power source regulator control of V3 pin: 0=Enable, generate USB power from 5V power source of VCC pin; 1= Disable; the USB power source can be externally inputted from the V3 pin	0
05H bit 1	Reserved	The data read is meaningless and must be 0	0
05H bit 0	BIT_CTRL_OSCIL_OFF	Clock oscillator control: 0=oscillation allowed; 1=oscillation stopped	0
06H	REG_USB_SETUP	USB configuration register	00000000
06H bit 7	It must be 1	The data read is meaningless and must be 1	0
06H bit 6	BIT_SETP_AUTO_SOF	Automatically generate SOF enable: 0=Disable; 1=Enable, send out SOF packet automatically	0
06H bit 5 06H bit 4	BIT_SETP_USB_SPEED	USB bus rate: 00=12Mbps in full speed mode; 11=1.5Mbps in low speed mode; Other value = disabled	00
06H bit 3 06H bit 2	BIT_SETP_RAM_MODE	Backup buffer application method: 00 or 01=disable the backup buffer; 10=the second buffer of continuous transmission, the synchronous flag is 1 and selected; 11=the second buffer area of continuous reception, the synchronous flag is 1 and selected;	00
06H bit 1 06H bit 0	BIT_SETP_BUS_CTRL	USB bus status control: 00=normal/idle; 01=UD+low UD-low (bus reset); 10=disabled; 11=UD+low UD-high (bus recovery)	00
07H	REG_INTER_EN	Interrupt enable register	11110000
07H bit 7 to 07H bit 2	Must be 111100	The data read is meaningless and must be 111100	111100
07H bit 1	BIT_IE_DEV_DETECT	USB device detection interrupt enable: 0=disabled; 1=enabled, output from INT# pin	0
07H bit 0	BIT_IE_TRANSFER	USB transmission completion interrupt enable: 0=disabled; 1=enabled, output from INT# pin	0
08H	REG_USB_ADDR	USB device address register	00000000
08H bit 7	Reserved	The data read is meaningless and must be 0	0
08H bit6 to 08H bit0	BIT_ADDR_USB_DEV	Address of USB device currently being operated	0000000
09H	REG_INTER_FLAG	Interrupt flag register, read only	X0X00000
09H bit 7	BIT_IF_USB_DX_IN	Sample status of UD+ pin at full speed/UD- pin at low speed: 0=low level/speed mismatch; 1=high level/speed match	X
09H bit 6	Reserved	The data read is meaningless	0

09H bit 5	BIT_IF_DEV_ATTACH	Current connection status of USB device: 0= no USB device is connected/ disconnected/ unplugged; 1= at least one USB device has been connected/ plugged in	=/X
09H bit 4	BIT_IF_USB_PAUSE	USB transmission pause flag, Effective in case of 1; write 1 to this bit to clear, This bit is automatically set to 1 after each USB transfer is completed	0/X
09H bit 3	BIT_IF_WAKE_UP	Chip wake-up completion interrupt flag, Effective in case of 1; write 1 to this bit to clear, This bit is automatically set to 1 after the chip wake-up is completed	0/X
09H bit 2	Reserved	The data read is meaningless	0/X
09H bit 1	BIT_IF_DEV_DETECT	USB device plug detection interrupt flag, Effective in case of 1; write 1 to this bit to clear, This bit is automatically set to 1 after detecting that the USB device is plugged or unplugged	0/X
09H bit 0	BIT_IF_TRANSFER	USB transmission completion interrupt flag, Effective in case of 1; write 1 to this bit to clear, This bit is automatically set to 1 after each USB transfer is completed	0/X
0AH	REG_USB_STATUS	USB status register, read only, Usually only querying after the corresponding interrupt is detected	1XXXXXXX
0AH bit 7	BIT_STAT_SIE_FREE	Status of current USB interface engine SIE: 0=busy/transmitting; 1=idle/waiting	1/X
0AH bit 6	Reserved	The data read is meaningless	X
0AH bit 5	Reserved	The data read is meaningless	X
0AH bit 4	BIT_STAT_TOG_MATCH	Indicate whether the current USB transmission is successful: 0= transmission failure; 1= transmission success and synchronization	X
0AH bit 3 to 0AH bit 0	BIT_STAT_DEV_RESP	Reply PID of USB device: 0010= transaction reply ACK of device for OUT/SETUP; 1010= transaction reply NAK of device for IN/OUT/SETUP; 1110= transaction reply STALL of device for IN/OUT/SETUP; 0011= transaction reply DATA0 of device for IN 1011= transaction reply DATA1 of device for IN XX00=device reply error or no reply in case of timeout; Other values = illegal response/accident	XXXX
0BH	REG_USB_LENGTH	USB length register, read only/write only, Read the receive length of the USB host,	XXXXXXXX

		Write the transmit length of the USB host,	
0CH	Reserved	Disable reading and writing	????????
0DH	REG_USB_H_TOKEN	USB host token register	========
0DH bit 7 to 0DH bit 4	BIT_HOST_PID_TOKEN	Specify transaction/token PID: 1101=SETUP transaction; 0001=OUT transaction; 1001=IN transaction; 0101=SOF packet; other values=disabled. Note: After the SOF packet is completed, there is no interrupt, and the SIE status can be queried	====
0DH bit 3 to 0DH bit 0	BIT_HOST_PID_ENDP	Specify the number of destination terminal to be operated: 0000 to 1111=terminal number 0 to 15	====
0EH	REG_USB_H_CTRL	USB host control register	00000000
0EH bit 7	BIT_HOST_RECV_TOG	Host receive synchronous flag: 0=DATA0; 1=DATA1	0
0EH bit 6	BIT_HOST_TRAN_TOG	Host transmit synchronous flag: 0=DATA0; 1=DATA1	0
0EH bit 5	Reserved	The data read is meaningless and must be 0	0
0EH bit 4	Reserved	The data read is meaningless and must be 0	0
0EH bit 3	BIT_HOST_START	Host transmission start control: 0=pause; 1=transmission enabled, automatically cleared to 0 after completion	0
0EH bit 2 to 0EH bit 0	Reserved	The data read is meaningless and must be 000	000
0FH-3FH	Reserved	Disable reading and writing	????????
40H-7FH	RAM_HOST_TRAN	USB host transmit buffer	========
C0H-FFH	RAM_HOST_RECV	USB host receive buffer	========
80H-BFH	RAM_HOST_EXCH	USB host backup buffer	========

6. Functional Specification

6.1. MCU Interfaces

CH370 chip supports general-purpose 8-bit passive parallel interface and SPI synchronous serial interface. During the power-on reset of CH370 chip, CH370 will sample the status of the CS#, WR# and RD# pins. If both WR# and RD# are at low level (grounded) and CS# is at the high (connected to the positive power source), select the SPI serial interface. Otherwise, select the parallel interface.

The interrupt request outputted by the CH370 chip INT# pin is active at the low level by default, and the MCU can learn the interrupt request of CH370 in the interrupt mode or query mode. To save pins, the MCU can directly query the interrupt flag register REG_INTER_FLAG of CH370 to learn the interrupt without being connected to the INT# pin of CH370.

6.2. Parallel Interfaces

The parallel port signal lines include: 8-bit bidirectional data buses D7～D0, read strobe input pin RD#, write strobe input pin WR#, chip selection input pin CS# and address input pin A0.

For the MCU similar to the Intel parallel port time sequence, the RD# and WR# pins of the CH370 chip can be connected to the read strobe output pin and write strobe output pin of the MCU respectively. For the

MCU similar to Motorola parallel port time sequence, the RD# pin of the CH370 chip shall be connected to the low level, and the WR# pin shall be connected to the reading and writing direction output pin R/-W of the MCU.

The following table shows the true values of the parallel port I/O operation (X in the table means that this bit is not concerned, and Z means that CH370 tri-status is disabled).

CS#	WR#	RD#	A0	D7-D0	Actual operation on CH370 chip
1	0	0	X	X/Z	Sampling is started for selecting SPI port mode during the power-on reset of CH370 chip
1	X	X	X	X/Z	CH370 is not selected, and no any operation is made
0	1	1	X	X/Z	Although selected, no any operation is made
0	0	1/X	1	Input	Write the index address to CH370, which is the starting address for subsequent reading and writing operations
0	0	1/X	0	Input	Write data to the specified address, and the index address will increase progressively after completion, facilitating continuous reading and writing
0	1	0	0	Output	Read data from the specified address. The index address will increase progressively after completion, facilitating the continuous reading and writing
0	1	0	1	Output	Read data from the specified address. The index address remains unchanged, facilitating the reading and writing back after modification

CH370 chip occupies two address bits. When the A0 pin is at high level, select the index address port, and you can write a new index address, or read data but keep the index address unchanged Select the data port when the A0 pin is at the low level. You can read and write the data corresponding to the index address, and automatically add 1 to the index address after the reading and writing operation is completed to facilitate the continuous reading and writing of the next data. The steps for the MCU to read and write to the CH370 chip through an 8-bit parallel port are: Firstly, write the index address from the index address port, and then read and write several data continuously.

The auto-increment of index address is only applicable to the buffer areas with address no less than 40H, and not applicable to registers with address less than 40H.

6.3. SPI

The SPI synchronous serial interface signal lines include: SPI chip selection input pin SCS#, serial clock input pin SCK, serial data input pin SDI and serial data output pin SDO.

The SCS# pin of the CH370 chip is driven by the SPI chip selection output pin or the general output pin of the MCU. The SCK pin is driven by the SPI clock output pin SCK of the MCU. The SDI pin is driven by the SPI data output pin SDO or MOSI, and SDO pin is connected to the SPI data input pin SDI or MISO of the MCU. For the hardware SPI interface, it is recommended that the SPI setting is CPOL=CPHA=0 or CPOL=CPHA=1, and the data bit sequence is MSB first.

The SPI interface of CH370 supports the MCU to simulate SPI interface for communication with the common I/O pins. The SDO of CH370 is a three-status output pin, which will only output after receiving a reading operation command. To save pins, the SDO pin of CH370 can be connected in parallel with the SDI pin and then connected to the bidirectional I/O pin of the MCU. It is recommended that the SDO pin of CH370 shall be connected to the SDI pin in series with a few hundred ohms.

The SPI interface of CH370 supports SPI mode 0 and SPI mode 3. CH370 always inputs data from the rising

edge of the SPI clock SCK, and outputs data from the falling edge of SCK when the output is allowed. The data bit sequence is MSB first, and 8 full bits are a byte.

Operation procedure of SPI:

① The MCU generates the SPI chip selection of CH370 chip, which is active at low level;

② The MCU sends out a one-byte address code according to the SPI output mode, which is used to specify the initial address of subsequent reading and writing operations;

③ The MCU sends out a one-byte command code to indicate the operation direction. The reading operation command code is C0H, and the writing operation command code is 80H;

④ For the writing operation, the MCU sends out one-byte data to be written, and CH370 receives and saves it to the specified address, and then, the address is automatically increased by 1. The MCU continues to send several bytes of data to be written, and CH370 processes them in sequence until the MCU disables the SPI chip selection;

⑤ For the reading operation, CH370 reads one-byte data from the designated address and the address is automatically increased by 1 after output. The MCU receives and saves the data. CH370 continuously reads the data from the next address and outputs it, until the MCU disables SPI chip selection;

⑥ The MCU disables the SPI chip selection of CH370 chip to end the current SPI operation.

6.4. Other Hardware

When CH370 chip works normally, 24MHz clock signal shall be provided for it externally. Generally, the clock signal is generated by the built-in inverter of CH370 through the externally applied 24MHz crystal stable frequency oscillation. If the 24MHz clock signal is inputted directly from the outside, it shall be inputted from the XI pin, and the XO pin is suspended.

CH370 chip supports supply voltages of 5V and 3.3V. When a 5V operating voltage is used, the VCC pin of the CH370 chip will input an external 5V power source, and the V3 pin shall be connected to an external power decoupling capacitor with a capacity of about 0.01uF to 0.1uF. When a 3.3V operating voltage is used, the V3 pin of the CH370 chip shall be connected to the VCC pin, and the external 3.3V power source will be inputted in the meantime.

7. Parameters

7.1. Absolute Maximum Value

Critical value or exceeding the absolute maximum value may cause the chip to work abnormally or even be damaged.

Name	Parameter description	Min.	Max.	Unit
TA	Ambient temperature during operation	-40	85	℃
TS	Ambient temperature during storage	-55	125	℃
VCC	Supply voltage (VCC connects to power, GND to ground)	-0.5	6.0	V
VIO	Voltage on the input or output pins	-0.5	VCC+0.5	V

7.2. Electrical Parameters

Test Conditions: TA=25℃, VCC=5V, excluding the pins connected to the USB bus.

(If the supply voltage is 3.3V, all current parameters in the table need to be multiplied by a factor of 40%)

Name	Parameter description		Min.	Typ.	Max.	Unit
VCC	Supply voltage	CH370T: V3 pin is not connected to VCC pin	4.5	5	5.3	V
		V3 pin connected to VCC pin	3.0	3.3	3.6	

ICC	Total supply current during operation	VCC=5V		5	25	mA
		VCC=3.3V		2	12	
ISLP	Supply current at the low power status I/O pin suspended/ internal pull-up	VCC=5V		0.07	0.15	mA
		VCC=3.3V		0.06	0.1	
VIL	Low level input voltage		-0.5		0.7	V
VIH	High level input voltage		2.0		VCC+0.5	V
VOL	Low level output voltage (4mA draw current)				0.5	V
VOH	High level output voltage (4mA output current)		VCC-0.5			V
IUINT	High-level pull-up output current of INT# pin		30	250	360	uA
IUP	Input current at the input terminal of other built-in pull-up resistor		3	150	250	uA
VR	Voltage threshold of power-on reset		2.1	2.5	3.0	V

7.3. Internal Timing Parameters

Test Conditions: TA=25°C, VCC=5V or VCC=3.3V

Name	Parameter description	Min.	Typ.	Max.	Unit
FCLK	Input clock frequency of XI pin	23.99	24.00	24.01	MHz
TPR	Internal reset time of power-on	14	25	40	mS

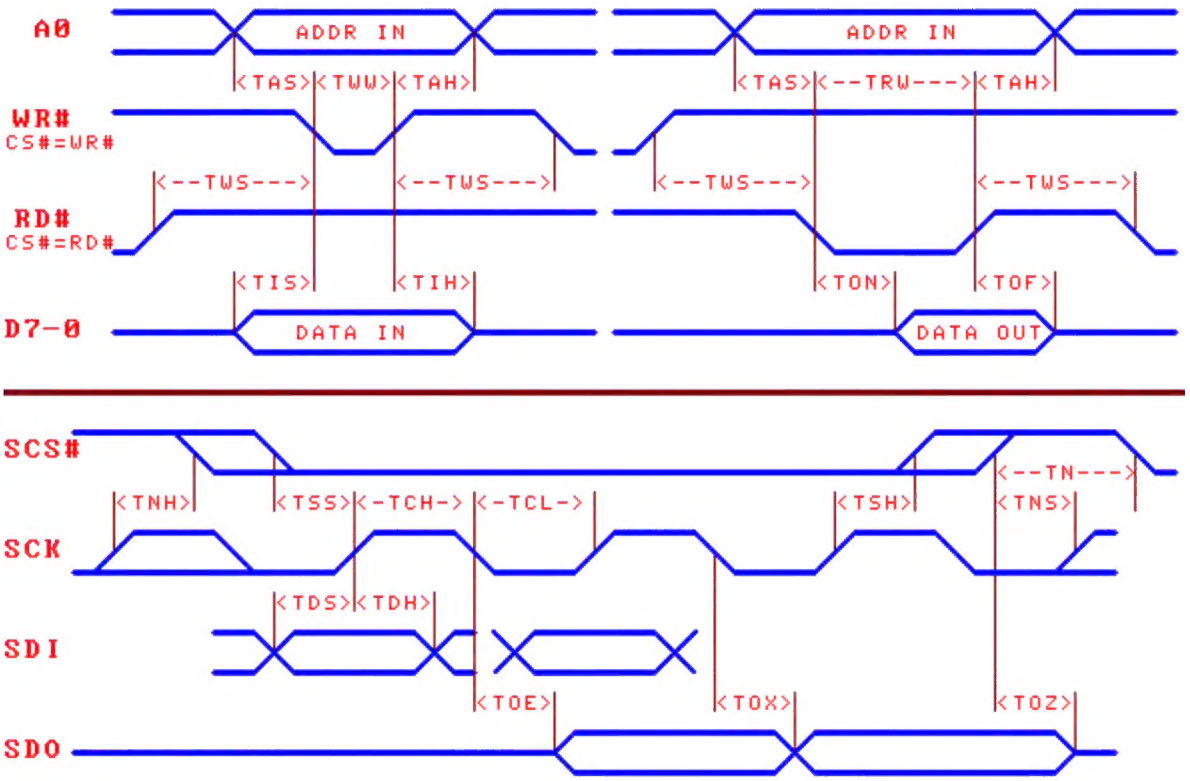
7.4. Parallel Port Timing Parameters

Test Conditions: TA=25°C, VCC=5V, the parameter in brackets VCC=3.3V, refer to the attached figure below

(RD means that the RD# signal is valid and the CS# signal is valid; WR#=1& RD#=CS#=0 performing a reading operation)

(WR means WR# signal is valid and CS# signal is valid, WR#=CS#=0 performing a writing operation)

Name	Parameter description	Min.	Typ.	Max.	Unit
TWW	Write pulse width	40 (50)			nS
TRW	Read pulse width	40 (50)			nS
TWS	Interval width of read strobe pulse or write strobe pulse	130 (150)			nS
TAS	Address input setup time before RD or WR	5 (7)			nS
TAH	Address input hold time after RD or WR	4			nS
TIS	Data setup time before Write HIGH	1			nS
TIH	Data hold time after Write HIGH	4 (6)			nS
TON	Read strobe RD valid to data output valid		20 (28)	30 (45)	nS
TOF	Read strobe RD invalid to data output invalid			22 (30)	nS



7.5. SPI Timing Parameters

Test Conditions: TA=25℃, VCC=5V. For the parameters in brackets, VCC=3.3V. Refer to the attached figure above.

Name	Parameter description	Min.	Typ.	Max.	Unit
TSS	Setup time of SCS# valid before SCK rising edge	20 (30)			nS
TSH	Hold time of SCS# valid after SCK rising edge	20 (30)			nS
TNS	Setup time of SCS# invalid before SCK rising edge	20 (30)			nS
TNH	Hold time of SCS# invalid after SCK rising edge	20 (30)			nS
TN	Time of SCS# invalid (SPI operation interval time)	90 (130)			nS
TCH	SCK clock high-level time	16 (20)			nS
TCL	SCK clock low-level time	20 (26)			nS
TDS	Setup time of SDI input before SCK rising edge	5 (7)			nS
TDH	Hold time of SDI input after SCK rising edge	3			nS
TOE	SCK falling edge to SDO output valid	2	14 (20)	20 (26)	nS
TOX	SCK falling edge to SDO output change		10 (14)	14 (20)	nS
TOZ	SCS# invalid to SDO output invalid			20 (26)	nS

8. Application

8.1. 5V Parallel Port Mode (Figure below)

This is the parallel port connection circuit of CH370. The VCC power source of CH370 chip in the figure is in 5V voltage.

Capacitor C3 is used for decoupling the internal power node of CH370. C3 is a monolithic or high-frequency ceramic capacitor with a capacity of 0.01μF to 0.1μF. Capacitor C4 is used for decoupling the external power source, and C4 is a monolithic or high-frequency ceramic capacitor with a capacity of 0.1μF.

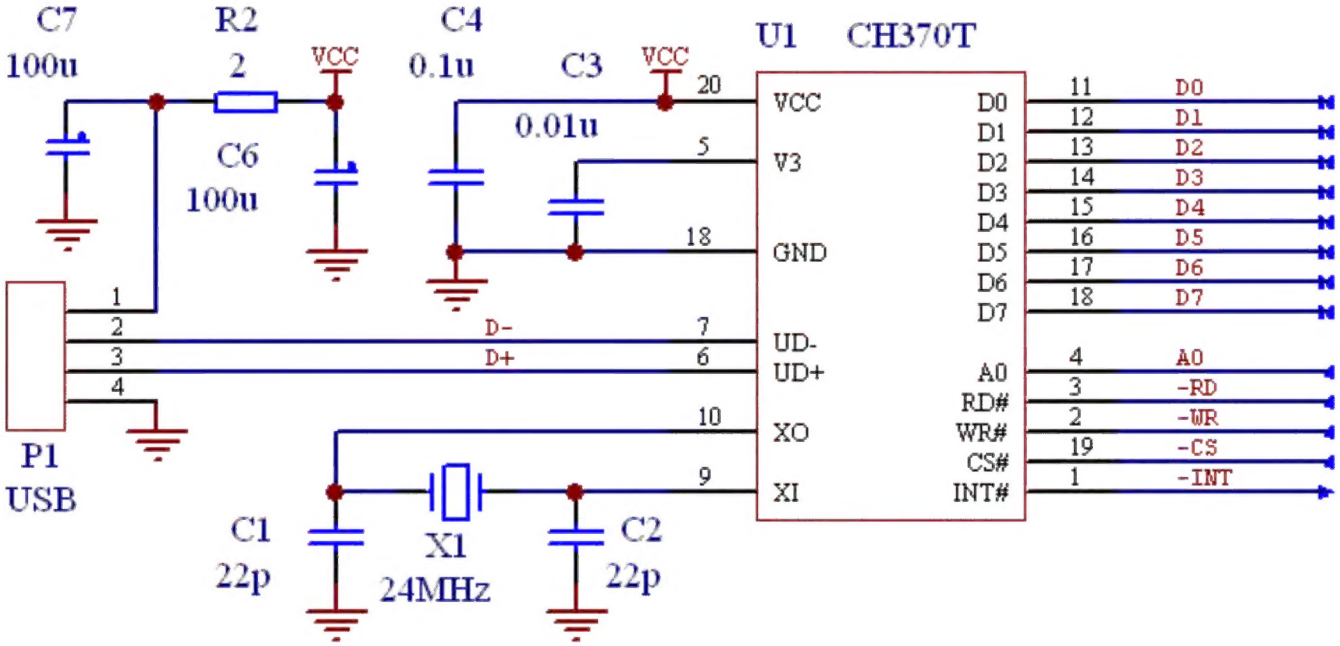
Crystal X1, capacitors C1 and C2 are used in the clock oscillation circuit of CH370.

It is recommended that the decoupling capacitors C3 and C4 shall be as close as possible to the connected pins of CH370 when the printed circuit board PCB is designed; the D+ and D- signal lines shall be close to parallel wiring, and ground wire or covered copper shall be provided on both sides to reduce the external signal interference; the length of the signal lines related to the XI and XO pins shall be shortened as far as possible to reduce the external interference of the high-frequency clock. The ground wire or covered copper shall surround the relevant components.

The resistor R2 and the capacitor C7 are used to limit the peak current when the USB device is just connected, and the resistor R2 can be replaced by a current limiting resistor or inductor.

If the interrupt request output pin INT# is not connected, the MCU program can also be replaced by querying the interrupt flag register.

The CH370 chip has a general-purpose passive parallel interface, which can be directly connected to a variety of MCUs, DSPs, MCUs, and CPUs through D0-D7, A0, -RD, -WR, -CS and -INT signals.



8.2. SPI Mode

If the RD# and WR# pins of the CH370 chip are at the low level (grounded) and the CS# pin is at the high level (connected to a positive power source), then CH370 will work in SPI serial port mode. In the SPI serial port mode, CH370 only needs to be connected to 5 signal lines with the DSP/MCU: SCS# pin, SCK pin, SDI pin, SDO pin, and INT# pin. Other pins can be left suspended.

To save pins, the INT# pin can be left unconnected, and the interrupt flag register can be queried instead, but

the query efficiency is low.

8.3. Operating Voltage 3.3V

If the VCC of the CH370 chip is 3.3V, then the V3 pin must be short-circuited with VCC to input 3.3V together, but the USB supply voltage provided to the external USB device should still be 5V.